ABSTRACT

A synchronous DRAM is provided having specified time slots (e.g., every multiple of 4 clock pulses of a DRAM input clock) within which read or write commands may be entered on the command/address bus. During operation, the DRAM performs internally generated refresh operations on a periodic basis while avoiding collisions with controller-generated data accesses. An internal refresh cycle can be executed without interfering with any data accesses by starting the refresh after decoding a non-conflicting command in one of these time slots and finishing before the next command time slot. If an internal refresh operation is delayed (e.g., by the decoding of a conflicting access command) it will be completed at the earliest opportunity thereafter.